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EXAMINER	
PAUL, ANTONY M	

ART UNIT	PAPER NUMBER
2837	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,934	DAIO ET AL.	
	Examiner	Art Unit	
	ANTONY M. PAUL	2837	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 thru 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 thru 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/12/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 2, 3, 8, 9 and 10 are objected to because of the following informalities: In regard to claim 1, the phrase, "output current detection transistor current-mirror" is not clear as to whether it's a transistor or current mirror circuit. In regard to claims 3, 8 and 9, the phrase, "predetermined terminal" is not explicitly taught in the specification. In regard to claims 2, 3 and 10, the phrase, "IC" needs to be in full form. Appropriate corrections are required wherever necessary.

Objection to Specification

2. The disclosure is objected to because of the following informalities: The phrase, "predetermined terminal" is not explicitly taught in the specification. Appropriate correction is required.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 4 thru 10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al. (US 7,079,368).

Claims:	**Ishikawa e t al. teaching:**
Claim 1: An over-current protection circuit of a semiconductor circuit including a power transistor for outputting current output,	Ishikawa et al. shows in fig. 1 an over current protection circuit such as a current restriction circuit 14 of a semiconductor driving circuitry 100 (fig.1, col. 1, lines 12-19), which includes a power transistor 10, which outputs a load current (load current supplied to the load 200, see figs.1, 2, 9; col. 2, lines 53-57),
a first output current detection circuit and	Fig. 1 shows a transistor 13 detecting load current flowing to the power transistor 10 (col. 3, lines 1-3),
a current limiter circuit for limiting the output current by stopping the output current of the power transistor for a predetermined period in response to a first detection signal from the output current detection circuit when the output current of the power transistor reaches a predetermined limit value, comprising:	A current limiter circuit such as a current restriction circuit 14 restrict current to the power transistor 10 based on the first detection signal such as the load current (incoming or load current, see figs. 2, 9) detected by the current detection circuit 13 is applied at the non-inverting input of the comparator 14a of said current limiter circuit 14. The output current such as the load current to the power transistor 10 is stopped associated with a predetermined time (T1 or T2) set by the timer 17 based on the load current reaching an over-current threshold (see col. 3, lines 1-16, 23-49, 55-60, col. 4, lines 52-67 & col. 5, lines 4-21 & 40-43).
an output current detection transistor current-mirror connected to the power transistor; and	The transistor 13 (fig.1) connected to the power transistor 10 is a current mirror circuit, which detects the load current outputted to the power transistor 10 (col. 3, lines 1-3), and
a second output current detection circuit for generating a second detection signal according to an output current of the output current detection transistor when the output current reaches a predetermined value larger than the	A second output current detection circuit such as the current restriction detection circuit 16 (detects the amount of current to the power transistor 10, see col. 3, lines 9-11) generate a current restriction detecting

predetermined limit value, wherein the output current of the power transistor is cut off for the predetermined period by operating the current limiter circuit in response to the second detection signal.	signal (see col. 4, lines 32-39, over-current restriction signal shown in figs 2-3) associated with the load current flowing to the power transistor 10 being detected by the transistor 13. The restriction signal (figs. 2-3) is generated based on comparison of the detected load output current exceeding an over-current threshold having predetermined value (first or second threshold, see col. 3, lines 38-48, 55-57, col. 4, lines 1-19 & 52-67), The load current outputted to the power transistor 10 is stopped using time period set by the timer 17 in response to the second detection signal such as the current restriction detection signal (figs. 2-3) outputted by the current restriction detecting circuit 16 associated with the current restriction operation by the current limiting circuit [14], which operates in response to the detected load current signal, over-current threshold signal applied at the inputs of the comparator 14a (see col. 3, lines 29-54 & col. 4, lines 52-67 & col. 5, lines 1-21).
Claim 2: The over-current protection circuit as claimed in claim 1, wherein the semiconductor circuit is a motor driver circuit IC, the predetermined value is set in a range within which a continuous drive of a motor by the power transistor is possible without any trouble.	Fig.1 shows a semi conductor driving circuit 100 (when formed on a chip, col. 8, lines 18-19), which drives a load 200 (motor, see col. 2, lines 48-53), Predetermined value is set in a range such as a first threshold, second threshold (col. 4, lines 1-19) and load 200 is continuously driven using the transistor 10 as the load current is controlled below the threshold (see col. 3, lines 38-42).
Claim 4: The over-current protection circuit as claimed in claim 3, wherein the current limiter circuit includes a comparator, the comparator compares the terminal voltage generated in the first resistor with a predetermined reference voltage and	Fig. 1 shows a current limiting circuit 14, which includes a comparator 14a, which compares a predetermined threshold voltage generated by a first resistor 15a with a voltage in proportion to the load current applied at the comparator 14a (fig. 1 shows resistors 15a, 15b, 15c of a

	threshold voltage determination circuit 15, see col.3, lines 1-3, 29-37, 43-49, col.4, lines 13-27, 52-67) and
generates an output signal for cutting off the output current for the predetermined period according to a result of the comparison and	Comparator 14a based on comparison as explained above generates an over-current restriction signal (see figs 2-3), which is detected by the current restriction detection circuit 16, which outputs a current restriction detection signal to stop the load current to the power transistor 10 via circuits (17, 18, 19), wherein the timer circuit 17 sets predetermined time T1 or T2 (see col. 5, lines 1-21, see explanation in claim 1).
the comparator compares a voltage signal generated according to the second detection signal with the predetermined voltage and generates the output signal according to a result of the comparison.	Comparator 14 compares a voltage signal generated in proportion to the load current signal (applied at the inverting input) with a predetermined threshold voltage signal (applied at the non-inverting input) and generates an over-current restriction output signal (figs. 2-3) based on said comparison. Load current signal is repeatedly detected and compared with the threshold signal at the comparator 14a and the operation is repeated (feedback operation is repeated, see col. 3, lines 43-54),
Claim 5: The over-current protection circuit as claimed in claim 4, further comprising a chopping pulse generator circuit and a timer circuit, wherein the predetermined period is a constant period, the timer circuit is actuated by the output signal to measure the constant period,	Fig. 7 shows a pulse generator 24, which generates pulse with predetermined width (see figs. 2-3, col. 7, lines 1-10, pulse width modulation, see col. 6, lines 17-22), constant time period T1 or T2 set by timer 17 (see figs 1, 2-3, 7), timer 17 is actuated based on the current restriction detection signal outputted from circuit 16 and timer 17 counts predetermined time T1 (see col. 3, lines 11-14, col. 6, lines 36-40),
the chopping pulse generator circuit generates a pulse every constant period set by the timer circuit and the power	Power transistor 10 is driven using pulse width control associated with time period set by the timer 17 (on/off, see col. 2, lines

transistor is ON/OFF controlled by the pulse.	53-62, col. 6, lines 17-22). The other limitations are explained above.
Claim 6: The over-current protection circuit as claimed in claim 3, wherein the output current is a sink current from an output terminal of the power transistor and the motor is driven by the sink current.	Power transistor 10 drives a motor load 200 and driving using a sink current is implemented in the load current supplied by said transistor 10, which is driven in an on/off manner.
Claim 7: The over-current protection circuit as claimed in claim 6, further comprising a second resistor provided between the output current detection transistor and a reference voltage line, wherein the power transistor and the output current detection transistor are N channel MOS transistors and the second detection signal is generated correspondingly to a terminal voltage in the second resistor.	A second resistor 15b of circuit 15 is provided between the current detection transistor 13 and the voltage threshold reference line such as the non-inverting input terminal of comparator 14a), Such as MOS power transistor 10, MOS current detection transistor 13 (see fig.1, col. 2, lines 55-58), Voltage threshold determination circuit 15 includes resistors 15a, 15b, 15c used to generate detection signals such as the first and second threshold voltage signals detected at the comparator 14a (fig.1, see col.4, lines 13-27).
Claim 8: The over-current protection circuit as claimed in claim 7, further comprising a transistor for detecting an over-current, which is turned ON when the terminal voltage of the second resistor exceeds a certain value, and a third resistor provided within the motor driver IC between the predetermined terminal and the comparator,	Fig. 1 shows a transistor 13, which detects current flow to the power transistor 10, which is turned on or off associated with the threshold voltage generated by the second resistor 15b of circuit 15 connected to the terminal (such as the non-inverting terminal of comparator 14a, wherein the threshold voltage going above or below a certain value depends upon the voltage applied at the inverting input terminal of said comparator 14a, see fig.1, col. 4, lines 13-31), A third resistor such as the resistor (reference not shown) connected between non-inverting terminal of comparator 14a and the predetermined terminal such as the circuit connecting path of circuit 15, which determines predetermined threshold voltage, wherein said resistor is within the driving circuit [100], which drives a motor

wherein the second detection signal is generated when the transistor is turned ON to generate a voltage higher than the predetermined reference voltage at a terminal of the third resistor.	load [200] (driving circuit 100 is formed on a chip, as explained in claim 2), A second detection signal such as a second threshold voltage is generated at the third resistor 15c of resistor group 15a-c associated with a transistor 15d being turned ON, wherein a first predetermined threshold is higher than the second threshold (see col. 4, lines 13-27).
Claim 9: The over-current protection circuit as claimed in claim 8, wherein the terminal of the over-current detection transistor at which a ground current is generated and a terminal of the second resistor connected to the reference voltage line are connected to the predetermined terminal.	A ground current is generated at the circuit path connecting ground (see fig. 1 ground portion connecting battery 1) to the terminal such as the circuit path connecting the ground current detection transistor 15d and a terminal such as the circuit path connecting second resistor (15b or 15c) is connected to the reference voltage line such as the non-inverting terminal of comparator 14a. Terminals such as the circuit paths of said current detection transistor 15d and said resistor (15b or 15c) connecting to the predetermined terminal is implemented as they are included in the voltage threshold determination circuit 15, which determines the predetermined first and second threshold voltages.
Claim 10: A motor drive circuit comprising the over-current protection circuit claimed in claim 9, wherein the semiconductor circuit is an IC.	driving circuit [100] is formed on a chip as explained in claim 2.
Claim 12: A semiconductor device comprising a motor drive circuit as claimed in claim 10	Fig. 1 shows a semiconductor load driving device 100 comprising a driver circuit [12] driving a motor load 200 (see claim 2).

Claim Rejections – 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being obvious over Ishikawa et al.

In regard to claim 3, the output current detection circuit includes a first resistor and connected to a predetermined terminal of the IC and the first detection signal is a terminal voltage generated in the first resistor.

Ishikawa et al. shows in fig.1, an output current detection circuit such as [14], which includes a resistor (reference not shown and is connected to the predetermined non inverting terminal of comparator 14a of the driving circuit 100) and also teaches a resistor (15a or 15b or 15 c) of circuit 15 generating a voltage threshold signal (first or second threshold voltage, see col. 4, lines 13-27) and is applied at the resistor (reference not shown) connecting the non-inverting input of the comparator 14a. Ishikawa et al. further teaches that a load 200 comprise a resistor and is provided external to the drive circuit 100. A resistor provided external or internal of a circuit depends upon the application and is a matter of design choice.

Ishikawa et al. differs from the claimed invention by not showing the predetermined value is in a range higher than the predetermined limit value by 5% to 10% of the predetermined limit value. It is obvious that setting a predetermined value in a range by 5% to 10% depends on the load, wiring (see col. 4, lines 9-12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for a predetermined value in a range of 5% to 10%, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al. as applied to claim 10, and in view of Matsunaga et al. (6,838,853).

In regard to claim 11, Ishikawa et al. shows in fig. 1 a motor drive circuit 100 as claimed in claim 10, wherein the output terminal of the power transistor 10 is connected to a motor load 200 (col. 2, lines 48-53).

Ishikawa et al. do not teach a stepping motor.

Matsunaga et al. teach a stepping motor 20 (fig.1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the stepping motor of Matsunaga et al. in the drive circuit of Ishikawa et al. because a stepping motor operate with low noise and vibration (col. 1, lines 20-22).

Information disclosure statement

Examiner acknowledges the receipt of prior art documents submitted on 03/12/2007.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTONY M. PAUL whose telephone number is

(571)270-1608. The examiner can normally be reached on Mon - Fri, 7:30 to 5, Alt. Fri, East.Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benson Walter can be reached on (571) 272-2227. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Antony M Paul/
Examiner, Art Unit 2837 12/17/2008

/BENTSU RO/
Primary Examiner, Art Unit 2837